Thermally Transparent Multiplexing of Superconducting Signals to Transmon Qubits

Alessandro Paghi, Giorgio De Simoni, Elia Strambini, Fabio Beltram, Lucia Sorba, and Francesco Giazotto

NEST, Scuola Normale Superiore and Istituto Nanoscienze-CNR, Piazza San Silvestro 12, 56127 Pisa, Italy.

Abstract: Time Division Multiplexing (TDM) of non-dissipative superconducting signals was demonstrated with an integrated hybrid semiconducting-superconducting demultiplexer operating up to several GHz at 50 mK without affecting the Transmon qubit temperature.

TDM of cryogenic signal lines is an emerging technique that can significantly reduce wiring overhead, shorten cooldown time, and increase the number of accessible I/O ports in cryogenic quantum computers (QCs) (Fig. 1a). In conventional architectures, N dedicated signal lines connect room-temperature electronics to N ports of the quantum processing unit (QPU) across multiple temperature stages. This approach imposes substantial constraints on system cost, space utilization, and thermal load, ultimately limiting scalability.

TDM of RF signal lines enables efficient multiplexing of control and readout signals for qubits, allowing multiple QPU ports to be addressed through a reduced number of physical lines. In a multiplexed architecture, a single RF line can be routed to the lowest temperature stage and shared among multiple qubits, such that $N = 2^n$ QPU ports can be accessed using only n control lines. Furthermore, TDM can be extended beyond conventional dissipative RF routing to the multiplexing of non-dissipative signals, such as supercurrents, using superconducting solid-state multiplexers. This approach enables intrinsically low-loss and low-power signal distribution directly compatible with cryogenic environments.

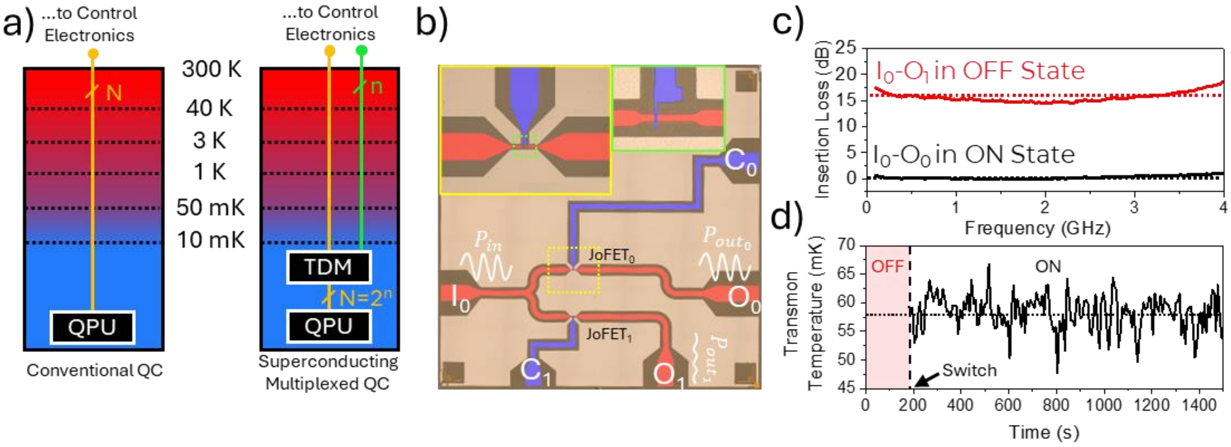

Fig.1 a) Conventional vs. superconducting multiplexed QCs. b) High-frequency hybrid demultiplexer with 1 input and 2 outputs. c) Insertion losses in the ON and OFF states. d) Transmon qubit temperature vs. switching events.

We report the TDM of superconducting signals using a voltage-actuated hybrid superconducting demultiplexer [1]. The device is fabricated on the InAs-on-Insulator (InAsOI) platform, consisting of an InAs epilayer grown on a cryogenic-insulating InAlAs metamorphic buffer, which enables electrical decoupling of adjacent surface-exposed devices and supports high critical-current-density integration [2]. The basic ON/OFF superconducting/resistive switching building is an InAsOI-based superconducting Josephson Field Effect Transistor (JoFET) [3]. InAsOI-based JoFETs feature Al as a superconductor and HfO_2 as a gate insulator, and they can entirely suppress the switching current and increase the normal-state resistance by 20 times in the gate voltage range [-4.5;0] V [3]. We proposed superconducting demultiplexers capable of operating in both low- and high-frequency regimes, with up to 8 routing outputs. To achieve high-frequency routing, a coplanar waveguide layout is employed, enabling efficient routing of superconducting signals up to 4 GHz with an ON/OFF ratio of 17.5 dB and no insertion losses in the superconducting state. The impact of the switching event on the temperature of a transmon qubit connected to the superconducting demultiplexer was evaluated. No temperature change is observed. This is a remarkable result compared to other techniques (e.g., electromechanical or cryo-CMOS switches) where hundreds of mK variations are observed, and power attenuators are required to suppress the thermal impact of the demultiplexer on the qubit temperature.

References

[1] A. Paghi *et al.*, "Supercurrent time division multiplexing with solid-state integrated hybrid superconducting electronics," *Nat. Commun.*, vol. 16, no. 1, p. 8442, Sep. 2025.

[2] A. Paghi, G. Trupiano, G. De Simoni, O. Arif, L. Sorba, and F. Giazotto, "InAs on Insulator: A New Platform for Cryogenic Hybrid Superconducting Electronics (Adv. Funct. Mater. 7/2025)," *Adv. Funct. Mater.*, vol. 35, no. 7, Feb. 2025.

[3] A. Paghi *et al.*, "Josephson Field Effect Transistors with InAs on Insulator and High Permittivity Gate Dielectrics," *ACS Appl. Electron. Mater.*, vol. 7, no. 9, pp. 3756–3764, May 2025.