A Hardware-Aware Approach to Quantum Computing in superconducting NISQ Processors

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Abstract: We present a hardware-aware approach for quantum computing, demonstrating the implementation of the first algorithms on Naples' public superconducting quantum computing center, analyzing real-device performance in the NISQ era.

Quantum computing is still in its early stages, although a tremendously fast advancement has been achieved in both theory and hardware in the latest years [1-4]. The development of quantum algorithms requires validation on real quantum processors to assess their practical performance under realistic conditions. However, current hardware platforms, while advancing quickly [5], are inherently affected by noise, and the roadmap towards fault-tolerant quantum computing is still long [6]. Despite this, quantum algorithms are often designed either assuming ideal fault-tolerant devices or relying on simulations with approximate noise models, which may not fully capture the behavior of real processors in the NISQ (Noisy Intermediate-Scale Quantum) era [7].

In this work, we first discuss on our strategy for hardware-aware quantum computing, the milestones and roadmaps to achieve an open and upgradable modular multi-node quantum computing system made of a 64-qubit superconducting Quantum Processing Unit (sQPU) ("Partenope") and a 25-qubit sQPU ("Ligea"). We demonstrate how the direct access of sQPU at the hardware level is beneficial to access the computational resources fundamentals for quantum advantage, to investigate the implementation of various quantum algorithms under realistic conditions, and to provide a tool to model noise in current NISQ processors and to understand limitations and advantages of quantum computing in the NISQ era [8,9].

Moreover, we focus on one use-case application in quantum finance, the Credit-Risk Analysis, through the Gaussian Conditional-Independence (GCI) model, one of the first algorithms run on the 25-qubit sQPU [10]. We demonstrate that hardware-aware quantum circuit transpilation based on a variational-like approach directly at the machine level allows us to overcome the limited connectivity and gate errors in our NISQ sQPU, with optimised outcome for such use-case.

Example References

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