Recent & future CMOS-SPAD developments at FBK

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Abstract: This talk reviews recent advancements in CMOS-SPAD technology at Fondazione Bruno Kessler, highlighting innovations in high-speed arrays and system integration. It also outlines the transition toward 3D-stacked architectures for scalable quantum imaging applications.

Quantum imaging techniques have demonstrated the ability to overcome classical optical limitations, enabling breakthroughs in super-resolution, sub-shot-noise, quantum ghost, and non-line-of-sight (NLOS) imaging. However, a significant gap remains between laboratory demonstrations using bulky optical setups and viable commercial exploitation. Single-Photon Avalanche Diode (SPAD) arrays in standard CMOS technology have proven highly effective at bridging this gap, integrating the functionality of large setups into millimeter-scale System-on-Chips (SoCs). This talk presents an overview of the recent advancements and future trajectory of CMOS-SPAD technology at Fondazione Bruno Kessler (FBK) in this domain.

A standout development is a 472×456 SPAD array for fast Quantum Ghost Imaging (QGI) calculating on-chip the photon correlations with a reference detector thanks to an in-pixel compensation for the electrical and optical delays. A smaller version of this architecture [1] was used by researchers at ICFO to demonstrate real-time waveguided QGI at video rates [2].

Expanding on system-level synchronization, FBK developed a two-channel module comprising two 32×32 single-photon image sensors [3], precisely synchronized via a primary FPGA generating a global time-base.

High-speed imaging was advanced with a fully digital 100×100 silicon photomultiplier (dSiPM) generating global photon counts at 10's of MHz rates over narrow time-gates, configurable down to 100 ps.

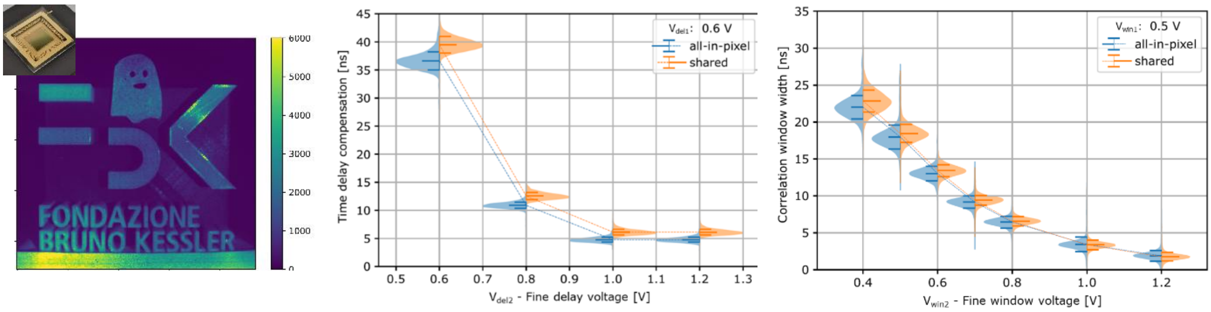

Fig. 1 (left) Intensity image acquired by the 472×456 imager for fast Quantum Ghost Imaging (QGI). (center and right) Characterization of the in-pixel delay lines aiming at the compensation of electrical and optical delays in the setup for coincidence detection with a bucket detector. Data refers to the reduced version of the array (10 kpixel).

Looking forward, FBK's roadmap focuses on miniaturization. A recent milestone is the development and preliminary characterization of a SPAD in a 22-nm FD-SOI CMOS process for integrated quantum random number generators (QRNG). Future developments prioritize 3D-stacked architectures, combining specialized sensing layers in FBK technology with advanced CMOS readout technology. This shift enables smaller pixel pitches, higher fill factors, and optimized sensitivity for real-time processing, serving as the foundation for future quantum imaging systems.

References

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[3] M. Zarghami et al., "A 32 × 32-Pixel CMOS Imager for Quantum Optics With Per-SPAD TDC, 19.48% Fill-Factor in a 44.64-µm Pitch Reaching 1-MHz Observation Rate," IEEE JSSC **55(10)**, 2819-2830 (2020)