Monolithic integrated platforms for single-photon SiN-based photonic circuits

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Abstract: We present recent progress on high-efficiency CMOS compatible solutions for a monolithic integrated photonic-circuit (SiN based, operated at 850nm) and single-photon detectors, fabricated on the same silicon chip, operating at room temperature.

An important topic in quantum photonics nowadays is the integration of single-photon detectors within the quantum PICs. Single-photon avalanche diodes (SPADs), particularly made in silicon, are good candidate because of their full CMOS compatibility and room temperature operation. We developed an efficient solution to realize a monolithic integration between SIN (conventional and quantum) photonic circuits PICs (operating at 850 nm) and the detectors (SPADs). The light coupling is based on a top-down convergence approach where the photons are evanescently coupled to the SPAD underneath, thanks to a modulation of the bottom cladding thickness and of the waveguide width at the SPAD location [1-3]. This approach is fully CMOS fabrication compatible, does not require alignments or butt-coupling, and operates the PIC and detectors at room temperature.

Following the first prototypes and demonstrator, we improved the fabrication process and manufactured two new lots of wafers: i) including different type of structures, with larger chip size and ii) improving the fabrication yield. Each chip has a moderately large area (0.5mm x 1mm) and includes photonic waveguides, couplers, modulators, etc, as well as monitoring diodes, and SPADs to detect the single photon at the end [3].

As further improvements, we focused on: i) an enhancement of the photon detection efficiency, and ii) further advancements in 3D integration. Concerning the former, given the long absorption length of 850nm photons, we focused on substrate thinning and wafer bonding, though an adhesive polymer. We realized the first PIC+detector with such approach. The goal is to have a reflection surface close to the epi-layer/substrate interface, to be able to reflect the photons exiting the WG but not absorbed by the photodetector. This increases significantly the effective absorption length, thus the detection efficiency. The later approach, instead, in towards a more aggressive integration of the system, and an improvement of the performance of the SPADs (particularly afterpulsing). We focused on 3D integration of the driving and control ASICs, for the photonic part and others for the SPADs. The silicon chip in this case will act as the PIC, with integrated detectors, as well as a routing carrier for the ASICs signals towards the PIC components and towards the outside world.

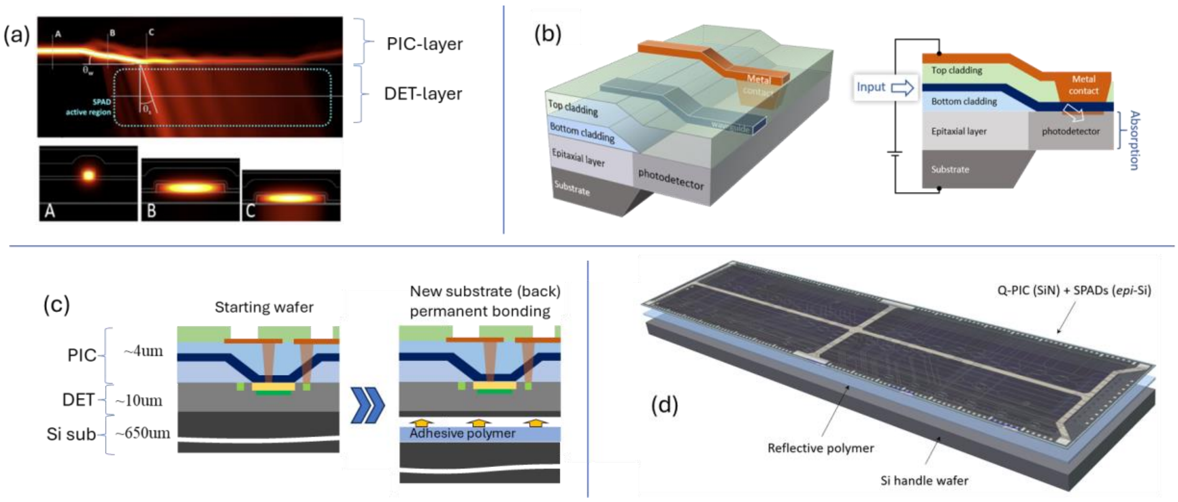

Fig. 1 Evanescent top-down coupling approach explained through a simulations of the field distribution in the WG (a), schematic representation of the chip structure in the detector coupling area (b), new approach to improve photon detection efficiency, towards substrate thinning, to increase effective absorption length (c) and (d).

References

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