Wiring Reduction in a Quantum Computer with On-Chip Time Division Multiplexing of Supercurrents

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Abstract: Time Division Multiplexing (TDM) of supercurrents was demonstrated with a 1-input-to-8-outputs superconducting demultiplexer operating up to 100 MHz at 50 mK employing InAs on Insulator (InAsOI), a new platform to develop hybrid superconducting electronics.

TDM of cryogenic signal lines is an innovative technique that can significantly reduce the required space, minimize the cooldown time, and increase the number of I/O ports of a cryogenic Quantum Computer (QC) (Figure 1a). In a traditional QC, *N* signal lines connect room temperature electronics to *N* ports of the Quantum Processing Unit (QPU) at low-temperature plates. These signal lines considerably impact the QC's costs, space utilization, and temperature stability. TDM of RF signal lines is an effective method for routing signals to the QPU. In a multiplexed QC, only one RF signal line is needed to reach the lowest temperature plate, allowing $N=2^n$ ports of the QPU to be connected using just *n* control lines.

Additionally, TDM can be applied to non-dissipative currents, such as supercurrents, alongside a non-dissipative superconducting solid-state multiplexer. This approach has the potential to extend the limits of traditional dissipative TDM. The advantages include but are not limited to: (i) shorter downtimes between control switching events, which enable faster port scanning; (ii) near-zero static power dissipation for energy savings; (iii) minimal heat and noise injection to support on-chip integration with the QPU; and (iv) reduced insertion loss.

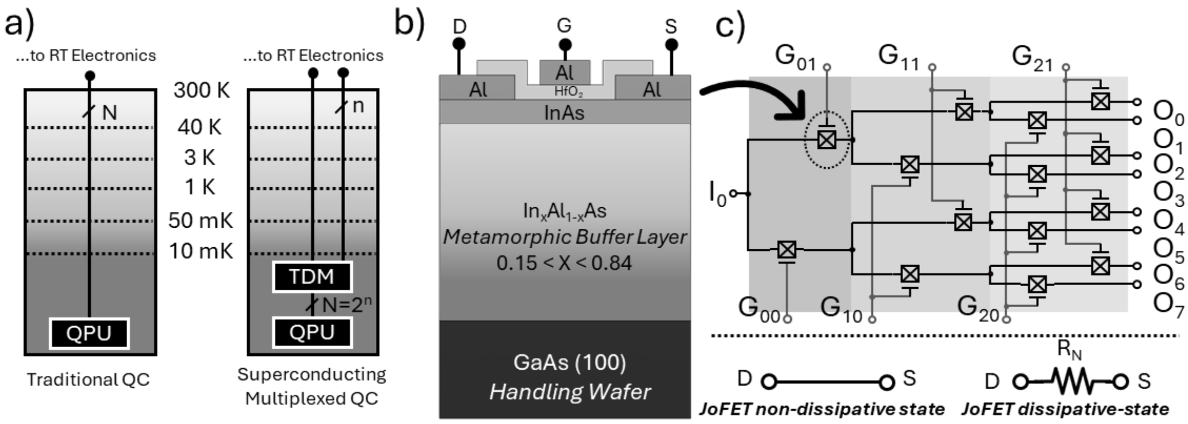

Fig. 1 a) Conventional vs. superconducting multiplexed QCs. b) InAsOI-based JoFET. c) InAsOI-based 1-input-8-outputs voltage-actuated hybrid superconducting demultiplexer with lumped element model of the JoFET.

For the first time, we report the TDM of supercurrent using a voltage-actuated hybrid superconducting demultiplexer [1]. The basic ON/OFF non-dissipative/dissipative building block is the InAs-on-Insulator (InAsOI)-based superconducting Josephson Field Effect Transistor (JoFET). InAsOI has been recently demonstrated as a promising platform to develop hybrid semiconducting-superconducting electronics. InAsOI consists of an InAs epilayer grown onto a cryogenic-insulating InAlAs metamorphic buffer, which allows the electrical decoupling of surface-exposed adjacent devices together with a high critical current density integration (Figure 1b) [2]. InAsOI-based JoFETs feature Al as a superconductor and HfO_2 as a gate insulator, and they can entirely suppress the switching current and increase the normal-state resistance by 20 times in the gate voltage range [-4.5;0] V [3]. The proposed superconducting demultiplexer features a hierarchical architecture, where 3 signal splitting levels are obtained involving 14 ON/OFF JoFETs integrated on the same chip and routed with Al traces, 1 input line (I_0), 8 output lines (O_0 to O_7), and 6 control lines (G_{00} to G_{21}) (Figure 1c). The superconducting demultiplexer operates up to 100 MHz at 50 mK, features an insertion loss of ~ 0 dB in the superconducting state, and an OFF/ON ratio of ~ 17.5 dB in a 50-Ohm-matched cryogenic measurement setup.

References

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[3] A. Paghi *et al.*, “Josephson Field Effect Transistors with InAs on Insulator and High Permittivity Gate Dielectrics Alessandro,” *Prepr. https//arxiv.org/abs/2412.16221*, 2025.