

## Impact of Parallel Gating on Gate Fidelities in Linear, Square, and Star Arrays of Noisy Flip-Flop Qubits Elena Ferraro<sup>1</sup>, Marco De Michielis<sup>1</sup>

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**Abstract**: Gate fidelities of linear, square, and star arrays of four flip-flop qubits are calculated to study the effect of noise, of idle qubits, and of parallel gating.

The achievable physical qubit error rate and the selected quantum error correction code determine how many physical qubits must be arranged in an array. Parallel gating, or the simultaneous manipulation of several qubits, is becoming an essential component of successful computation as the number of qubits in the array increases. A reliable assessment of the increase in gate infidelity induced by parallel gating needs to be considered for an accurate estimation of errors in Quantum Error Correction codes, enabling fault-tolerant quantum computation.

Small arrays of flip-flop (FF) qubits, a particular kind of donor-quantum dot-based qubits [1, 2], are examined in this work. To investigate the impact of parallel gating, simulation results of gate fidelity in linear, square, and star arrays (LA, SA, STA) of four FF qubits affected by realistic 1/f noise are presented. By comparing various array geometries, the effect of two, three, and four parallel one-qubit gates, as well as two parallel two-qubit gates, on fidelity is computed. The findings can contribute to the optimized manipulation of small FF qubit arrays and the design of larger ones [3, 4, 5, 6].



**Fig. 1** Infidelity of all configurations in the LA (green circles), SA (cyan squares) and STA (magenta stars) as a function of the number of parallel a) Rz ( $-\pi/2$ ) b) Rx ( $-\pi/2$ ) and c)  $\sqrt{i}$ SWAP gate(s) when  $a_{\Delta Ez} = 50$  V/m. The dashed lines connect points representing the average infidelity values over different configurations for each number of parallel operations.

## References

[1] G. Tosi, F. A. Mohiyaddin, V. Schmitt, S. Tenberg, R. Rahman, G. Klimeck, A. Morello, "Silicon quantum processor with robust long-distance qubit couplings", Nat. Comm. **8**, 450 (2017).

[2] R. Savytskyy, T. Botzem, I. F. de Fuentes, B. Joecker, J. J. Pla, F. E. Hudson, K. M. Itoh, A. M. Jakob, B. C. Johnson, D. N. Jamieson, A. S. Dzurak, A. Morello, A., "An electrically driven single-atom flip-flop qubit", Science Advances **9**(6), 9408 (2023).

[3] E. Ferraro, D. Rei, M. Paris, M. De Michielis, "Universal set of quantum gates for the flip-flop qubit in the presence of 1/f noise", EPJ Quantum Technology **9**, 1-11 (2022).

[4] D. Rei, E. Ferraro, M. De Michielis, "Parallel Gate Operations Fidelity in a Linear Array of Flip-Flop Qubits", Adv. Quantum Technol. **5**, 2100133 (2022).

[5] M. De Michielis, D. Rei, E. Ferraro, "Parallel Gate Fidelity of Flip-Flop Qubits in Small 1D-and 2D-Arrays in a Noisy Environment", Adv. Quantum Technol. **7**, 2300455 (2024).

[6] M. De Michielis, E. Ferraro, "Impact of Parallel Gating on Gate Fidelities in Linear, Square, and Star Arrays of Noisy Flip-Flop Qubits", Adv. Quantum Technol. 2400341 (2024).